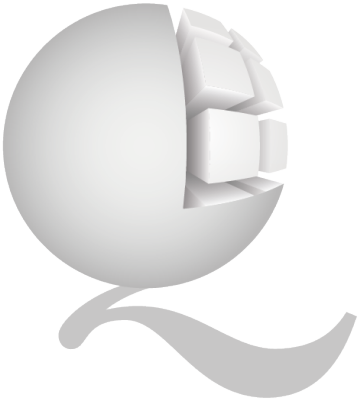
Horizon Europe Programme (2021-2027)
EIC Pathfinder Open
HORIZON-EIC-2022-PATHFINDEROPEN-01



QUADRATURE

Scalable multi-chip architectures enabled by cryogenic wireless/quantum-coherent network-in-package [†]

D1.1: Cryogenic antenna model

Contractual Date of Delivery	31/05/2024
Actual Date of Delivery	31/05/2024
Deliverable Dissemination Level	Public
Editor	Peter Haring Bolivar (U. Siegen)
Contributors	U. Siegen, UPC
Quality Assurance	Fabio Sebastino (TU Delft), Edoardo Charbon (EPFL)

[†]This project is supported by the European Commission under the Horizon Europe Framework Programme with Grant agreement no: 101099697.

Document Revisions & Quality Assurance

Deliverable Number	D1.1
Deliverable Responsible	U. Siegen
Work Package	WP5
Main Editor	Peter Haring Bolivar (U. Siegen)
Contributors	Eduard Alarcon (UPC), Fátima Rodríguez (UPC)

Internal Reviewers

1. Fabio Sebastiano (TU Delft)
2. Edoardo Charbon (EPFL)

Revisions

Version	Date	By	Overview
1.3.0	31/05/2024	*Peter Haring Bolivar (U. Siegen)*	Final release.
1.2.0	24/05/2024	*Peter Haring Bolivar (U. Siegen)*	Integration of improvements suggested by the quality reviewers (EPFL, TUD) and internal revision.
1.1.0	20/05/2024	*Eduard Alarcon (UPC)*	First draft.

Legal Disclaimer

Executive Summary

The vision of the QUADRATURE project aims to explore and validate a new generation of scalable quantum computing architectures featuring distributed quantum cores interconnected via quantum-coherent qubit state transfer links and orchestrated via an integrated wireless interconnect, thereby supporting architectural reconfigurability to serve massive flows of heterogeneous quantum algorithmic demands. Among the objectives, on the lower end of the quantum full stack, the project targets to experimentally achieve the transfer of classical data through the wireless in-package links enabled by integrated antennas at deep cryogenic temperatures, co-integrated with cryo-RF transceivers, capable of short-distance operation (10cm) with high data rate (2 Gbps).

In this context, this report explores the feasibility and provides alternative designs for an on-chip miniaturized antennas that will enable future wireless channels characterization, will be co-integrated and will co-exist with the cavity-enabled quantum channel. The document reports in revisiting miniaturizing antennas in wireless-network-on-chip and in-package scenarios, with the uniqueness of cryogenic operation of materials and packages. The report culminates with designing and assessing performance of several candidate antenna topologies.

Abbreviations and Acronyms

AIN Aluminum Nitride

BW Bandwidth

CT Cryogenic temperature

EM Electrimagnetic

MCMC Many-Core Multi-Chip

NoCs Networks-on-Chip

PEC Perfect Electric Conductor

QC Quantum Computing

RF Radio frequency

RT Room temperature

SiO_2 Silicon Dioxide

TSV Through-Silicon-Vias

WNoC Wireless Networks-on-Chip

The QUADRATURE consortium is composed by

UPV	Coordinator	Spain
UPC	Beneficiary	Spain
TU Delft	Beneficiary	Netherlands
UoS	Beneficiary	Germany
UNICT	Beneficiary	Italy
EQUAL1	Beneficiary	Ireland
BSC CNS	Beneficiary	Spain
NUID UCD	Beneficiary	Ireland
EPFL	Associated partner	Switzerland

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1. Introduction

1.1 Organization of the report

This report first provides a state of the art revision and context for miniature antennas integratable on chips within pacakages, highlighting their benefit in networks-on-chip scenarios as in QUADRATURE, to enable wireless-on-chip brodcast function for synchronization and temporal orchestration. The report then evluates operation of miniaturized antennas within computing packages, including the effect of antenna location within the packaged chip, given the enclosed reverberant condition of the package cavity. The document then elaborates on a design-oriented methodology for cryogenic antennas in a quantum computer enclosed package, and proposes alternative designs by studying performance in the form of field distribution and S paramenters characterizations, both for dipole and bowtie antenna topologies.

2. Miniature Antennas

In this section, we aim to provide insights into the challenges and requirements to be faced when designing antennas for size and resource-constrained scenarios with high-performance demands, namely, a multicore processor.

2.1 Networks-on-Chip (NoCs)

Networks-on-chip consist of a fabric of on-chip routers and has been the *de facto* standard for the interconnection of cores in the last decade. Packets are injected into the network by the processor core of the source node and received by the processor core of the destination node through several intermediate nodes [4].

The NoCs paradigm works reasonably well for a few cores, however, as we enter the hyperscaling era their limited scalability and mediocre latency when connecting distant cores, turns, again, communication into the performance bottleneck of many-core systems, thus calling for solutions at the interconnect level [3, 7].

2.2 Wireless technology: a possible alternative

The Wireless Network-on-Chip paradigm arises as one of the alternatives to alleviate some of the performance limitations of NoCs. WNoCs consist of the integration of Radiofrequency (RF) front-end with cores or clusters of cores [12] and are generally thought to complement a wireline NoC rather than to replace it.

Radio waves from a transmitting antenna propagate through the chip, nearly at the speed of light, and at a given frequency until reaching the intended destinations, also located within the same package. [1, 20].

WNoC offers multiple benefits. For instance, low latency is achieved because intermediate router hops are avoided, moreover, the data propagates close to the speed of light over the electromagnetic waves in the package. This also enables broadcast support, when using omnidirectional antennas, for multiple, simultaneous, and faster communication links. Besides, the absence of wires in WNoC provides flexibility as opposed to wireline NoC which is fixed and heavily overprovisioned to cover all possible applications of a certain architecture.

However, the limited sizes of nanodevices makes it difficult to apply classical EM communication paradigms. Moreover, material behavior at the nanoscale is mainly unexplored and could lead to wrong design assumptions [13]. Miniaturization of antennas to meet the chip scale size requirements imposes very high communication frequencies. Many on-chip antennas like meander dipole, zigzag dipole, slot, loop, inverted F, bow-tie and Yagi have been designed and investigated [2, 5, 10, 11, 15, 22, 23]. The main requirements for on-chip antennas are that they have to be compact and have

multi-gigahertz bandwidth to sustain the required data rates of many-core multi-chip (MCMC) systems [15].

3. Antennas in Computing Packages

The objective of this section is to cover important aspects of the integration of a miniature antenna in a computer package.

3.1 Computing packages

The antenna design and channel evaluation depend on a good characterization of the landscape, otherwise, the results of the WNoc execution might be unrealistic and overly optimistic. The propagation of the electromagnetic waves in this enclosed environment is ruled by the same phenomena that affect its homologous large-scale scenario. This means that within the chip, the EM waves will suffer reflections and scattering when reaching an obstacle, as well as diffraction when bending at the edges of the chip. Some of the waves will be absorbed at a certain distance when propagating through a material; and refraction when traveling between mediums with different refraction indexes.

A computer chip is formed by stacking layers of metal separated by dielectrics [14]. Depending on the integration approach considered, there are several ways of connecting a chip with the rest of the system. A widely used package nowadays, that constitutes the baseline of our work is the flip chip. The structure is made stacking layers of copper and dielectric. From top to bottom, the layers are heat sink and heat spreader, both to dissipate the heat of the structure because of their thermal conductivity. It then follows the silicon die, made of bulk silicon for the operation of transistors. The material of this layer is harmful to the electromagnetic propagation around the package. The insulator layer is made of silicon dioxide (SiO_2), and separates the silicon die from the interconnect layers, which are made of copper [14].

Table 3.1: Package parameters.

Parameter	Thickness	Materials	Units
Heat Spreader	0.5	Aluminum Nitride	mm
Silicon die	0.5	Bulk Silicon	mm
Lateral Space	0.5	Vacuum	mm
Chiplet insulator	0.01	SiO2	mm
Bumps	0.0875	Copper	mm
Frequency	60	-	GHz

The detailed structure of a representative flip-chip package can be seen in Figure 3.1 In this configuration, the chips are turned over and connected to the system substrate through a set of solder bumps. The packaged chip therefore has the silicon substrate on top, which is in turn interfaced by the spreader material and system heat

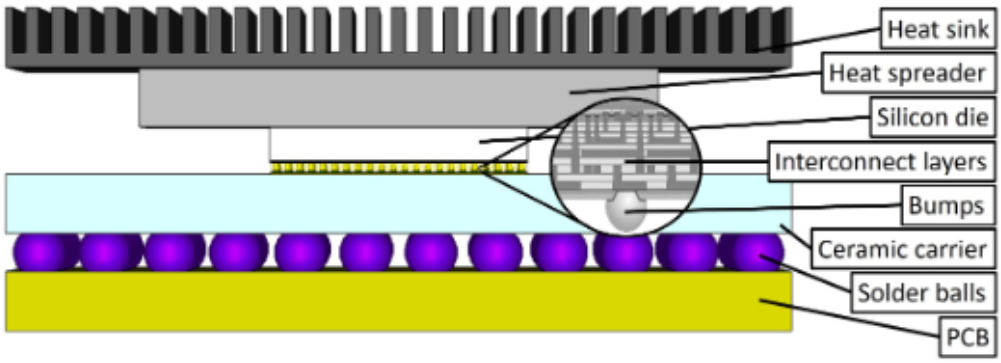


Figure 3.1: Schematic of the layers of a flip-chip package [20]

sink on top. The insulator and metal stack are placed at the bottom, interfaced by the solder bumps that connect it to the system [6, 21].

3.2 Antenna location in the chip

The antenna placement is a main design decision, specially in this highly integrated environment. The antenna position in the chip affects the location of the excitation ports which is important on the channel characterization. The flip-chip package does not leave much space for the location of antennas. Some works propose to place the element as far as possible from the silicon, though this is unrealistic in a flip chip package because the antenna will be short-circuited by the array of micro-bumps. Antennas such as patches and printed dipoles might be implemented in the metal layers close to the silicon. However, the proximity to the virtual ground plane formed by the array of micro-bumps reduces their efficiency, whereas co-planarity between antennas further increases losses [21]. An alternative is to fabricate Through-Silicon Via (TSV) to implement vertical monopoles [17, 21].

Placing the antennas vertically in the chip, either on top of the substrate or coming out of it has an important size constraint. This scenario has a height limitation of a few um or less, so for an antenna of $\lambda/4$ to fit this requirement it must have an operation frequency of over 300 GHz if it radiates in air or vacuum. This, of course, changes if the antenna is embedded in the dielectric. For the same wire length, antenna resonant frequencies would decrease proportionally to the dielectric refractive index if the antenna and wireless link are embedded within a dielectric. Placing them horizontally gives space for larger metalic structures, however, one must be cautious because they still need to be small enough to fit many of them within the chip. Horizontal wires may be more easily fabricated as printed antennas, and these can be generalized to a number of planar structures such as patches, meander or folded dipoles [8, 9, 18]. Planar antennas on-chip dominate the literature, however, their radiation pattern is broad, which means they radiate upwards and away from the chip instead of the desired omnidirectional radiation towards a receiving antenna. Since size is a largely important parameter in this environment, aperture antennas, despite their high gain, are generally prohibitive. In [16] a zigzag monopole antenna is proposed to resonate in the 60 GHz band, placed within the insulator. However, they considered a simple chip environment without any heat sink which is typical of this environment.

4. Cryogenic Antennas in Package

In this section, we present the assumptions regarding materials and geometries for the design of a cryogenic antenna at 28 GHz (as specified in former deliverable D2.1 devoted to RF transceiver self-specification) and its subsequent integration into a quantum package. The preliminary channel exploration and characterization has considered using a monopole antenna. Furthermore, we explore the behavior of other two antenna designs in free space and in the quantum package. These models are dipole and bow-tie.

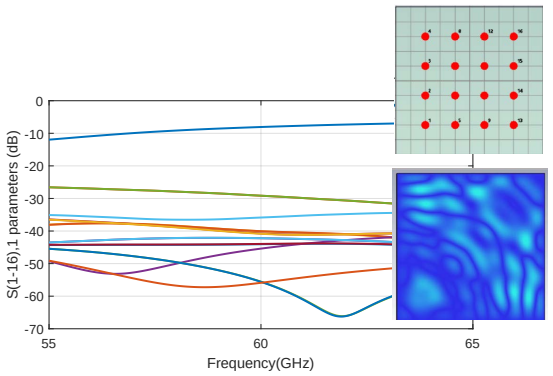
4.1 Methodology

We start building from our experience, by simulating a flip-chip package as described in Section 3.1 and observing the influence of cryogenic temperatures in the wireless channel.

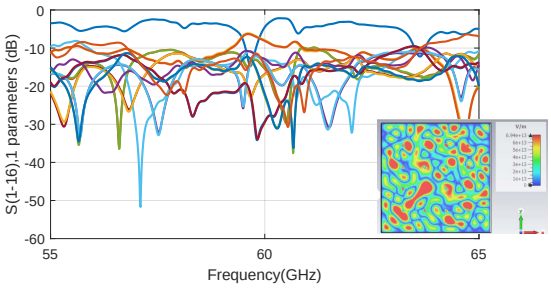
The flip chip is also surrounded by a metallic enclosure. This converts the wireless channel into a reverberation chamber. The energy will bounce around the structure and create notches in the channel response in frequency and time. However, since all the architecture, node placement, and geometry are known beforehand and remain static after implementation, we have the leverage of having an almost deterministic and invariant channel. This knowledge allows an accurate pre-characterization of the channel, easing the compensation tasks of the channel impairments.

For this setting, we compare the channel and the EM propagation for a flip chip at room temperature and the same structure at cryogenic temperatures. Since CST does not take into account temperature when simulating, we must model the behavior at cryogenic temperatures by modifying the characteristics of the materials. Low temperatures influence the electric conductivity and the losses of the materials, while the electromagnetic parameters (permittivity and permeability) remain almost constant. Some representative metals such as aluminum and niobium will become superconductive at cryogenic temperatures. Regardless if the metal becomes superconductive or not, low temperatures have a positive impact on its electric conductivity. Therefore every metal for the structure at 4 Kelvin will be modeled as a perfect electric conductor (PEC). Low temperatures also influence the amount of losses experienced by the structure, For this, dielectrics will be modeled as lossless materials. This approach is not entirely accurate but it provides a fair enough approximation with low computational costs. To perform the EM propagation, we use 16 monopole antennas placed through the silicon and feed from the metal layers below.

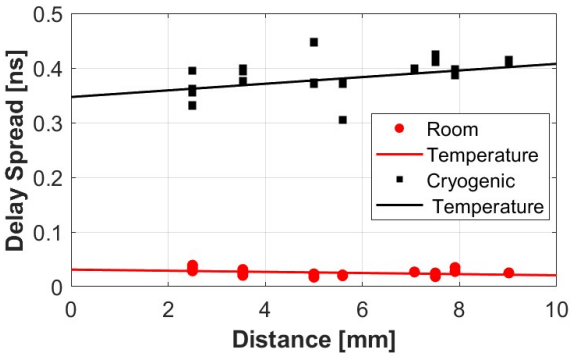
In Figure 4.1 we can see the difference in the behavior for both setups. It is clear that, for room temperatures, the channel will be less notchy, thanks to the lossy nature of the bulk silicon, that absorbs a large portion of the radiation paths. This makes for



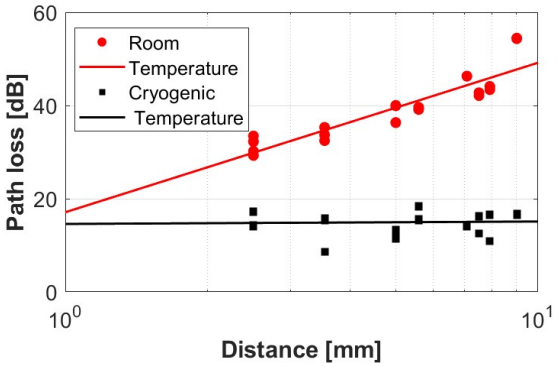
(a) Channel and EM field, room temperature.



(b) Channel and EM field, cryogenic temperatures.



(c) Delay spread



(d) Path losses

Figure 4.1: Channel behavior and characterization at room and cryogenic temperatures

low delay spread but a largely attenuated channel leading to a power deficit in transmission. The opposite occurs when considering the materials as perfect conductors or with negligible losses. The channel becomes notchy and enlarges due to the large amount of propagating paths bouncing on the structure. In this case, we deal with a reverberant channel with low path losses but enlarged due to the delay spread. In figures 4.1a and 4.1b we can see insets of the EM field for both temperatures. This field distribution matches with what is inferred from the S parameters. In the lossy material. the landscape is almost blue with a small amount of waves going around the geometry. In the other case, we find many spots of field concentration because of the reverberant nature and low path losses given by low temperatures.

This approach has allowed us to have first-hand knowledge of the behavior of the channel at cryogenic temperatures. When moving to a quantum package design, it is expected that the wireless channel will behave qualitatively similarly, with quantitative differences in performance would be due to changes in gemotries.

4.2 Quantum package design

Once we know what to expect when transmitting in an almost-perfect environment we proceed to model a geometry of the quantum package based on the structure presented in the proposal, see figure 4.3.

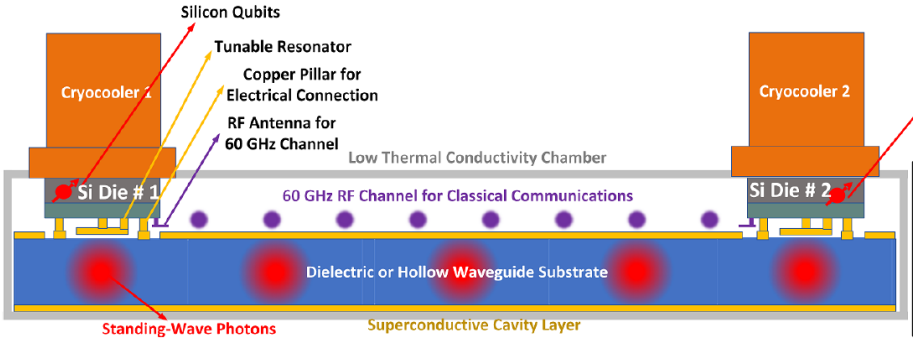


Figure 4.2: Proposal of the quantum cavity

The system requirements for the transceiver design define a carrier frequency of operation of 28 GHz. We adopt this frequency for our wireless channel design. The monopole antenna that was used at 60 GHz is reusable since the new frequency is approximately a harmonic and will radiate properly. The superconductive waveguide for the qubit transmission will be modeled as a PEC cavity filled with vacuum. We do this to have a more realistic model of the desired behaviour, however, our priority at this stage is the wireless channel characterization, and we focus on that. Also, isolating the qubit from the channel reverberance is one of our major concerns and we address this with some changes in the design. To simulate transmission at cryogenic temperatures, we repeat the methodology explained in the previous section, and model every material as lossless.

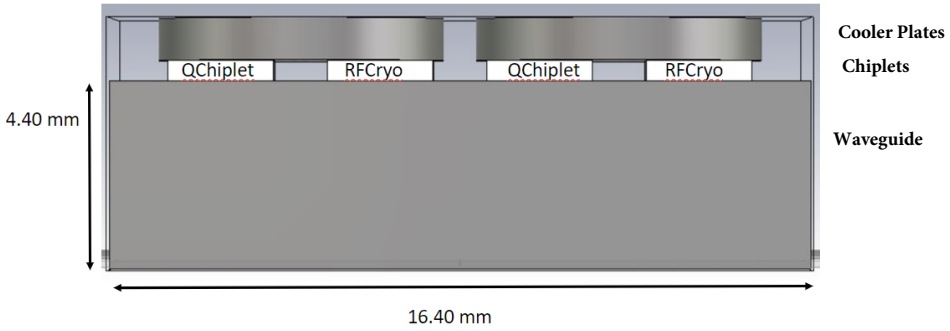
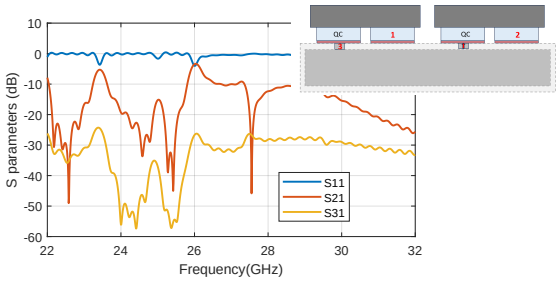


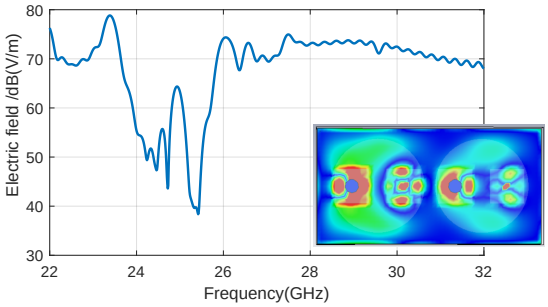
Figure 4.3: Proposal of the quantum cavity

The system structure and related geometries simulated in CST can be seen in Figure 4.3. Though this is not seen in the figure, the whole structure is surrounded by a metal cavity filled with vacuum, that covers the chiplets and a portion of the cooler plates. From top to bottom, we have metallic cooler plates (PEC). Next to the chiplets, based on the flip chip structure, there are two layers, one of silicon, and the other of (SiO_2), both lossless. The last layer represents the superconductive waveguide. Under each cooler plate, we have two chiplets. One of them is exclusively dedicated to passing the qubits to the waveguide (Qchiplet). The other (RFCryo) is augmented with the monopole antenna and used for wireless transmission. In Figure 4.4a, we see the detailed location of the antennas used for the measurements. Antennas 1 and 2 are used for classical wireless communication, and antenna 3 is placed in the aperture to measure the electromagnetic (EM) leakeage caused by antenna 1.

Right under the QChiplet, there is an opening that connects to the inside of the waveguide, which is used for the qubits state transfer. We place an antenna in the aperture, to measure how the wireless channel radiation will affect the QChiplet, see Figure 4.5a, in which the antenna in the opening is represented by number 3 in the aperture where the measurements were made, and by a red arrow in the other quantum chiplet.



(a) S parameters: S21 between antennas, S31 in the aperture



(b) EM field in the aperture.

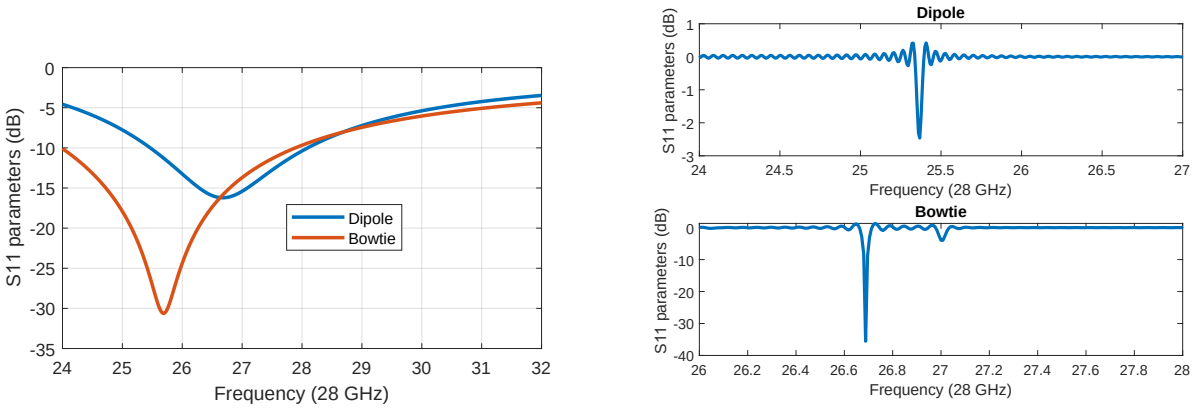
Figure 4.4: EM data of the structure

The S parameters shown in Figure 4.4a prove that when the RF antenna radiates, the energy that reaches the aperture is low, and we seem to have decent isolation values. Moreover, we place a field probe in the aperture to check the amount of EM field that is leaking towards the waveguide see Figure 4.4b. Our results conclude that there is a notable isolation between the QChiplets and the classical wireless channel. However, since the qubits are exhibit a remarkable fragility in front of the sorrounding environment, these values might not suffice and can jeopardize the entire system, thus this requiring further characterization in the future.

4.3 Antenna Results

In this section, we discuss the performance of two antenna designs inside an environment comparable to one with cryogenic temperatures. This is done by embedding the antennas in a box of lossless silicon surrounded by PEC. The antennas are first designed to resonate in free space and later tuned to resonate within the material properties.

In Figure 4.5a, we can see both designs radiating in free space in the desired frequency band with good values of reflection coefficient. However, once they are encased in silicon and metal the return losses shift a bit, see Figure 4.5b, and the resonance frequency changes while still being within the same band. Notches in frequency are also present though they are not visible in the image. These notches are a consequence of an environment low in losses and rich in multipath due to the nature of the materials. Managing the effects of reverberance while still achieving radiation and isolation for the qubits is our main challenge. We want to add that introducing the antennas in the quantum package proposal will lead to even more reflections and notches that will be appreciated in the S parameters and will be more similar to the observed in Fig 4.4a. Despite the channel complexity, it is still deterministic and almost invariant in time. Geometry, materials, and node location will be fixed, known, and will



(a) Antennas in free space.

(b) Antennas enclosed

Figure 4.5: Antenna resonance in different environments

remain the same after fabrication This knowledge arms us with the tools required to study and compensate the channel impairments [19] in future work.

5. Conclusions

This report has explored the feasibility and provided alternative designs for on-chip miniaturized antennas that will enable future wireless channels characterization, will be co-integrated and will co-exist with the cavity-enabled quantum channel. The work has revisited the approach for miniaturizing antennas in wireless-network-on-chip and in-package scenarios, while exploring the uniqueness of cryogenic temperature range operation of materials and packages. The report presents cryo-antenna design candidates, both in free space and enclosed in silicon, and assess performance in the form of field distribution and S parameters characterizations, both for dipole and bowtie antenna topologies.

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